IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **Toshio TAKAYAMA, et al.** Group Art Unit: **Not Yet Assigned**

Serial No.: **Not Yet Assigned** Examiner: **Not Yet Assigned**

Filed: **December 16, 2003**

For: **SEMICONDUCTOR DEVICE HAVING A MULTILAYER INTERCONNECTION STRUCTURE AND FABRICATION PROCESS THEREOF**

PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Date: December 16, 2003

Sir:

Prior to calculation of the filing fee and examination of this application, please amend the above-identified patent application as follows: